## CLAIMS

What is claimed is:

1. A testing system, comprising:

a tester including an oscillator with a first frequency;

a load board including an oscillator with a second frequency;

an error detector coupled to the tester and the load board, wherein the error detector generates an error signal proportional to the difference between the first and second frequencies and the error signal is used to vary the second frequency.

2. The system of claim 1, wherein the second frequency is variable.

3. The system of claim 1, further comprising a first divider coupled between the tester and the error detector and a second divider coupled between the tester and the error detector.

4. The system of claim 3, wherein the first and second dividers provide the error detector with common unit frequencies.

5. The system of claim 4, wherein the error signal is provided to the oscillator on the load board to vary the second frequency.

6. The system of claim 5, wherein the load board further comprises a device under test (DUT) that receives the second frequency.

7. The system of claim 5, wherein the first frequency $f_1$ and the second frequency $f_2$ are synchronized according to the equation $n \cdot f_1 = m \cdot f_2$, where $n$ and $m$ are integer numbers.

8. The system of claim 5, wherein the oscillator on the load board is a voltage controlled crystal oscillator.

9. The system of claim 1, wherein the error detector is an XOR gate.

10. A method of synchronizing a tester, comprising:

providing a first frequency from the tester;

providing a second frequency from a load board;

comparing the first and second frequencies; and

generating an error signal that is proportional to a difference between the first and second frequencies;

wherein the comparing generates a result that is used to vary the second frequency.

11. The method of claim 10, further comprising varying the second frequency.

12. The method of claim 10, further comprising dividing the first and second frequencies.

13. The method of claim 12, wherein the first frequency $f_1$ and the second frequency $f_2$ are synchronized according to the equation $n \cdot f_1 = m \cdot f_2$, where $n$ and $m$ are integer numbers.

14. The method of claim 13, further comprising utilizing the first and second frequencies as references for external components.

15. A testing system, comprising:

a load board including at least one DUT; and

a tester including:

an oscillator having an oscillation frequency;

a first divider coupled between the oscillator and the at least one DUT;

a second divider coupled to the oscillator; and

a phase locked loop (PLL) coupled between the second divider and the at least one DUT.

16. The testing system of claim 15, wherein the first divider provides a frequency divided version of the oscillation frequency to the at least one DUT.

17. The testing system of claim 15, wherein the PLL provides a synthesized version of the oscillation frequency to the at least one DUT.

18. The testing system of claim 15, wherein the first and second dividers have different divide ratios.

19. The testing system of claim 18, wherein the oscillation frequency of the oscillator $f_1$ and the frequency from the first divider $f_2$ are synchronized according to the equation $n \cdot f_1 = m \cdot f_2$, where $n$ and $m$ are integer numbers.

20. The testing system of claim 18, wherein the oscillation frequency of the oscillator $f_1$ and the frequency from the PLL $f_2$ are synchronized according to the equation $n \cdot f_1 = m \cdot f_2$, where $n$ and $m$ are integer numbers.

21. The testing system of claim 19, wherein the first and second oscillation frequencies are provided as references to external devices.

22. A method of synchronizing a tester, comprising:

generating a first frequency with the tester;

dividing the first frequency by various divide ratios to generate a plurality of frequencies;

synthesizing at least one of the plurality of generated frequencies;

providing the plurality of generated frequencies and the at least one synthesized frequency to a DUT;

wherein the first frequency is synchronized to both the plurality of generated frequencies and to the at least one synthesized frequency.

23. The method of claim 22, further comprising providing the plurality of generated frequencies and the at least one synthesized frequency to an external component.

24. A testing system, comprising:

a multiplexer;

a plurality of oscillators coupled to the multiplexer;

a plurality of dividers coupled to the multiplexer; and

a PLL coupled to at least one of the plurality of dividers;

wherein the testing system selects among the oscillators by configuring a selector on the multiplexer.

25. The testing system of claim 24, wherein the PLL synthesizes an oscillation frequency of the selected oscillator.

26. The testing system of claim 25, further comprising a DUT that receives the synthesized frequency from the PLL and also receives a divided frequency from at least one of the plurality of dividers.

27. The testing system of claim 26, wherein the synthesized frequency received by the DUT $f_1$ and the oscillation frequency of the selected oscillator $f_2$ are synchronized according to the equation $n \cdot f_1 = m \cdot f_2$, where $n$ and $m$ are integer numbers.

28. The testing system of claim 27, wherein the oscillation frequency of the selected oscillator is used as a timing reference for the testing system.

29. The testing system of claim 24, wherein the oscillator is a crystal oscillator.